A Highly Integrated Multi-Functional Chip Set For Low Cost Ka-Band Transceiver

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Abstract

This paper presents the development of a highly integrated multi-functional chip set for low-cost Ka-band transceiver. The transmitter portion consists of a 17.5-to-35 GHz doubler macrocell which delivers > 20 dBm of output power, a Ka-band SPDT polarization switch macrocell with > 45 dB of isolation and a > 10-W high power module. The receiver portion consists of a Ka-band doubler macrocell, an InGaAs/InAlAs/InP HEMT Ka-band balanced LNA with 1.9 dB noise figure and 19 dB gain and a Ka-band image rejection mixer with > 32 dB image rejection and 5.5 dB conversion loss. The high power module consists of two power modules; each can deliver 6-W with 24% PAE and an associated power gain of 21.5 dB [1]. The power module consists of a driver amplifier and two power amplifier chips. These MMIC amplifiers were fabricated with a 2-mil thick substrate using 0.15-μm InGaAs/AlGaAs/GaAs HEMT technology. The total GaAs real estate required for implementation of a typical pulsed-FM transceiver as shown in Figure 1 is < 150 mm^2. This highly integrated chip set will also reduce the assembly cost substantially.

Introduction

This multi-functional transceiver chip set addresses the needs of low-cost millimeter-wave (MMW) transceivers for smart weapons and phase array applications. Smart weapons operating at mmW frequencies reduce the susceptibility to jamming. The advantages of using monolithic microwave integrated circuit (MMIC) technology are cost reduction, better reliability, weight and size reduction without sacrificing high performance. Figure 1 shows a block diagram of a typical pulsed frequency modulated (pulsed-FM), polarization switchable transceiver. The LO input to the receiver and the input of the transmitter are derived from a VCO. The FM modulation sweeps the VCO to determine the range of the target.

Each polarized received signal is amplified by a Ka-band LNA and is downconverted to the IF signal by an image-reject mixer. The low noise characteristic of InGaAs/InAlAs/InP HEMT offers the advantage of superior noise figure. The image-rejection mixer provides an image rejection of > 32 dB and eliminates the need of an image rejection filter. This mixer has the flexibility of providing either lower-sideband (LSB) or upper-sideband (USB) conversion.The LO signal was derived from the doubler output and is fed 90° out of phase into the I and Q arms of the receiver chain. The IF signals are then amplified by the IF amplifiers and go to the IF signal processor, which provides range and position target information.

The transmitter consists of a K-band doubler macrocell, a pre-driver amplifier, a polarization switch macrocell and a high power amplifier module. The doubler macrocell amplifies the low phase noise input signal to 20 dBm and feeds the signal into the pre-driver amplifier. The x2 macrocell has a calibration port which taps a small amount of power and sets a calibration reference for the receiver. The pre-driver amplifier puts out 28 dBm to drive the rest of the power amplifier chain into compression for low output power variation over temperature. The polarization switch controls which output port, elevation or azimuth, is transmitting. The outputs of the 6-W power modules are shown to be combined through a wave-guide quadrature combiner. The system may be operated under pulsed or CW conditions.

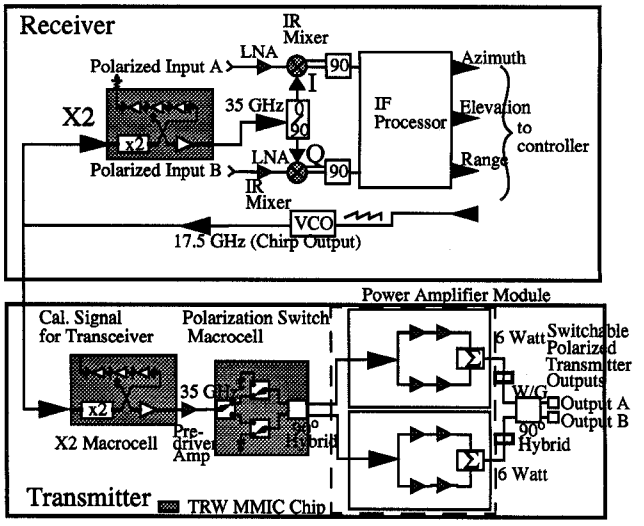

Figure 1. A Block Diagram of a pulsed-FM Transceiver

LOW NOISE AMPLIFIER (LNA)

Figure 2 shows the photo of the 2-stage InP HEMT LNA. This is a balanced two-stage design featuring 80 μm devices in the first stage and 200 μm devices in the second stage fabricated on TRW 0.15 μm InP HEMT process. The balanced topology provides good input VSWR for the receiver antenna output. InP technology provides superior noise figure and higher gain devices and is ideal for the LNA implementation. The on-wafer measured noise figure is 1.9 dB with an assocated gain of > 19 dB at Ka-

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band. The input return loss of the LNA was measured to be > 17 dB and the output return loss was > 20 dB. The measurment shown in Figure 3 were taken from 10 sites and the gain and noise figures were tightly grouped together.

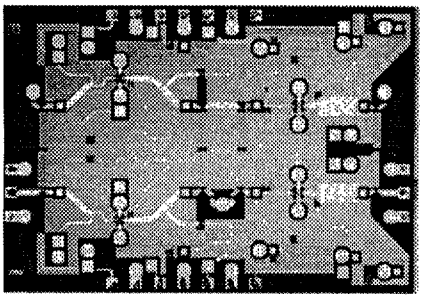

Figure 2. Photo of the LNA, 3.5x2.45mm^2.

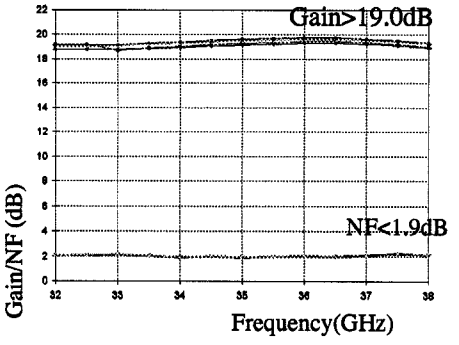

Figure 3. Measured Gain and Noise Figure of LNA.

IMAGE REJECTION MIXER

In a typical heterodyne system, it is often desirable to reduce signal corruption by its image. An image rejection filter is required in the system to eliminate the image. For a low IF system, it is very difficult to implement an image reject filter that can provide sufficient image rejection, and increasing the IF frequency can relax the image rejection requirement but will make it difficult to implement a high Q channel select filter at higher IF frequency. One solution to this dilemma is to replace the image rejection filter with an image rejection mixer. The image-rejection shown in Figure 4 is made up of two ratrace singly-balanced mixers, with LO fed in phase and RF fed 90 degree out of phase into the mixers.

The LO in phase power divider is a Wilkinson divider and the RF 90° hybrid is a Lange coupler. The IF outputs are connected to an off-chip 90° hybrid to provide either USB or LSB IF signal. The ratrace hybrid provides good LO-RF isolation through 180° phase separation between the LO and RF ports. The balun also provides phase cancellation of the LO signals at the IF ports, thus ensuring good LO-IF isolation. The measured performance of the mixer is shown in Figure 5 with 5 dB of conversion loss at 15 dBm LO power. The measured RF return loss was 10 dB. The LO-RF and LO-IF isolation were measured to be 29 dB and 31 dB respectively.

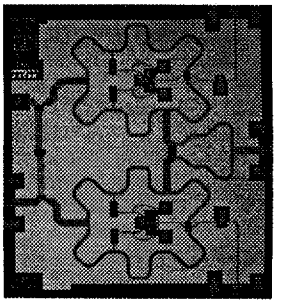

Figure 4. Photo of the Image Rejection Mixer, 2.6x2.7 mm^2.

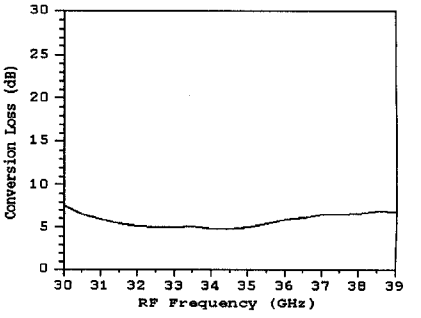

Figure 5. Measured Performance of the Singly-Balanced Mixer

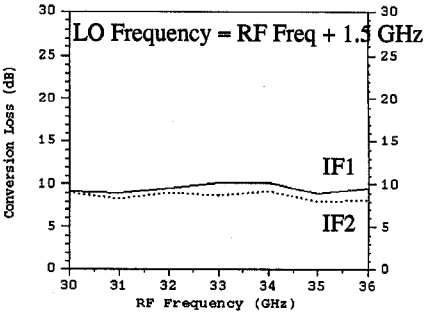

Figure 6. Measured Performance of the Image Reject Mixer without IF 90° hybrid

Figure 6 shows the measured data of the image-rejection mixer with 9 dB conversion loss at 17 dBm LO power. The true conversion loss after the 90° IF hybrid should be 5.5 - 6 dB. The image rejection measured at 1.5 GHz IF is 32 dB. This is superior to using an image rejection filter which provides about 17 dB image rejection for a compatible system. To reduce the GaAs real estate, the ring of the ratrace were folded inward to form a "petal-like" shape, the diodes and the matching networks were placed inside of the ring. The total chip area is 2.6x2.7mm^2.

DOUBLER MACROCELL

This chip (Figure 8), as shown in its block diagram in Figure 7, is made up of three major pieces: the single-ended active doubler, the buffer amplifier for the main RF output and the chain of amplifiers and attenuators for the calibration output.

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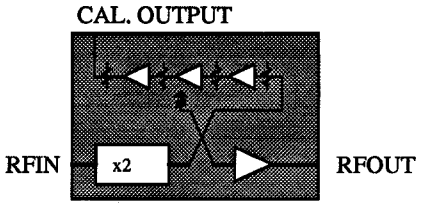

Figure 7. Block Diagram of the X2 Macrocell

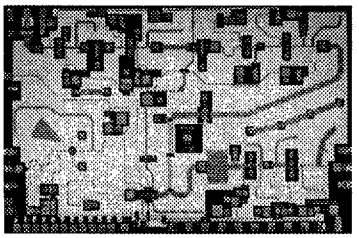

Figure 8. Photo of the X2 Macrocell, 4.3x2.8 mm^2.

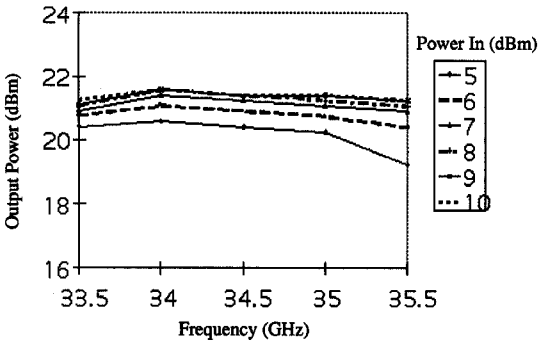

Figure 9. Measured Performance of the X2 Macrocell.

The active doubler features a 120 µm device. There is a second harmonic rejection radial stub at the input and a fundamental frequency rejection open stub at the drain for improved doubling efficiency. The output power is split between the buffer amplifier and the chain of amplifiers for the calibration output. When the main RF output is on (5 V is applied to the drain voltage) and the calibration output is off (0 V drain voltage) the buffer amplifier was measured providing at least 21 dBm in fixtured chip tests with 8 - 10 dBm of input power. The fixtured measurements are shown in Figure 9. Typical input return loss of the X2 was measured 15 - 20 dB with input power of 10 dBm. The RF functional yield for this macrocell cell is 67%.

With the main RF output off, the calibration output provides a constant output of about 10 dBm when the input power is from 5-10 dBm. The measured on/off isolation from the calibration port is greater than 60 dB. The chip size is 4.3 x 2.8 mm^2.

POLARIZATION SWITCH

Figure 10 shows the photo of the polarization switch. The polarization switch provides the quadrature power-split signals to drive the power amplifiers. The design employs a SPDT circuit with two HEMT shunt switches on each branch. The SPDT design is very similar to [2], employing two HEMT switches on each branch, with a nominal 1/4 wave stub between the main RF line and the HEMT switches. A third HEMT on each branch is used to switch on or off a resistance to provide a matched termination on the "off" branch of the SPDT switch. A quadrature branchline splitter provides the desired two equal amplitude power split RF outputs with 90 degree phase difference. The sign of the relative phase of the two signals is determined by which branch of the SPDT switch is turned "on".

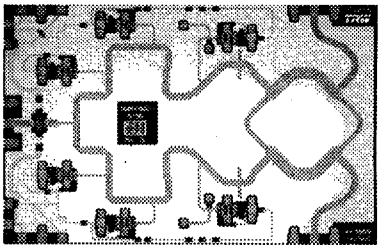

Figure 10. Photo of the SPDT Polarization Switch, 3.8x2.5 mm^2.

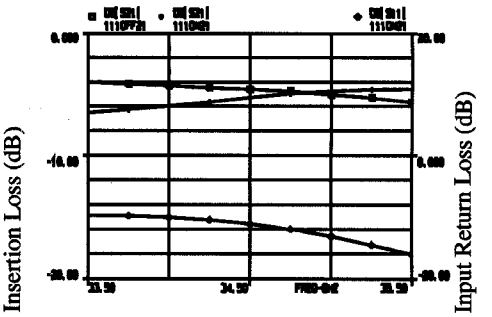

Figure 11. Ka-Band Polarized Switch Measured Results.

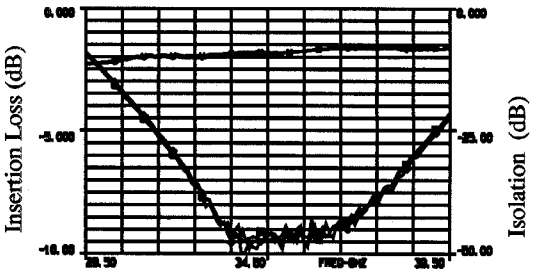

Figure 12. Measured Insertion Loss and Isolation of the Terminated SPST Switch.

Measured switch performance in the range of 33-36 GHz is 1.4 dB insertion loss (4.7 measured minus 3 dB power split) and a 5 degree phase imbalance at mid-band. Note that due to wafer probe testing limitations, chip measurements were taken with one of the two output ports open-circuited, rather than terminated in a matched load. Simulations indicated that this would cause up to a 2dB p-p ripple in the insertion loss and up to +-10 degrees phase error. Thus, error associated with the lack of a termination on the output port appears to be largely responsible for the deviation between wafer test measured results and the original design.

As a further check on the design, a SPDT switch without the quadrature splitter was also tested. The chip shows a peak isolation of > 42 dB at 33 GHz. Insertion loss was approximately 2 dB, close to the simulated value.

POWER AMPLIFIER MODULE

The high power module consists of two 6-W power modules[1]. Figure 13 shows the photo of the test fixture of the high power module. The outputs of these two modules will be combined through a wave-guide quadrature combiner. The projected saturated output power output of this module should be > 10-W.

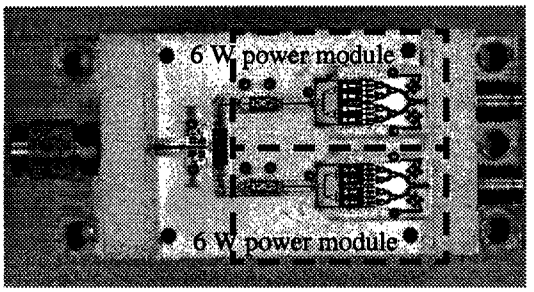

Figure 13. Photo of the High Power Module

The 6-W power module [1] consists of a driver amplifier and two power amplifier chips. These MMIC amplifiers were fabricated with a 2-mil thick substrate using 0.15-μm InGaAs/AlGaAs/GaAs HEMT technology. The driver amplifier is a fully matched single-ended design with an output power of 28.5 dBm, a > 8.5 dB power gain and 26% PAE. We use a hybrid approach for the output power amplifier which consists of two partially-matched MMIC chips and a 8-way Wilkinson combiner fabricated on Alumina substrate. The MMIC power amplifiers delivered an output power of 35.4 dBm (3.5W) with a PAE of 28% and an associated power gain of 11.5 dB. The power delivered per GaAs area is > 235 mW/mm^2 and the power density is > 520 mW/mm of device periphery. The 4-way input power splitter has a measured insertion loss of 0.4 dB and the 8-way output combiner has a measured insertion loss of 0.6 dB. The yield histograms for these chips were also reported in [1]. Figure 14 shows the measured performance of the entire power module including its coaxial interfaces (K-connectors) with an ouput power of 37.8 dBm(> 6-W) and PAE of 24% and an associated gain of 21.5 dB at mid-band.

These power MMIC chips can also be re-configured to produce a > 3 watt per channel power module for phase array applications by connecting a 4-way Wilkinson combiner to one PA chip.

Conclusion

We have developed a complete highly-integrated compact MMIC chip set for an ultra low noise (< 1.9 dB N.F. for the front-end LNA) and high power (>10 W) Ka-Band FMCW transceiver. The power delivered per GaAs area is > 235 mW/mm^2 and the power density is >520 mW/mm of device periphery. The total GaAs real estate required for the entire transceiver is < 150 mm^2.

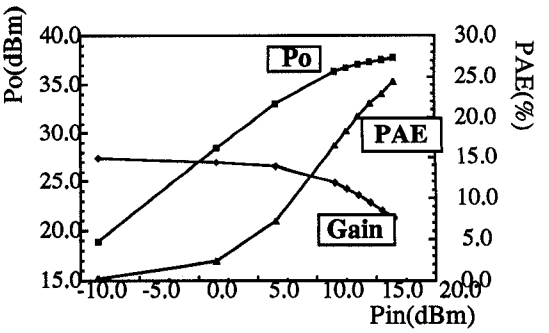

Figure 14. Measured in-fixture performance of the 6 Watt power module [1]

Acknowledgements

The authors would like to thank W. Yamasaki, L. Callejo and B. Gorospe for test support, C. Geiger for processing the wafers. We appreciate the valuable inputs of Barry Allen, Mike Aust and Mark Dufault who served in the design review teams. We would also like to thank Ernie Holmes for his valuable discussions on the system architecture. The power MMIC development was supported in part by the DARPA Amy Research Laboratory under MAFET Thrust II program. The rest of the tranceiver components development was supported by TRW Internal Research and Development Fund.

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